REMARKS/ARGUMENTS

In conjunction with the filing of a Request for Continued Examination, and response to the final Office Action dated September 8, 2003 and the Advisory Action dated January 28, 2004, claims 1 and 11 are amended. Claims 1, 2, and 4-13 remain in the application. It is not the Applicant's intent to surrender any equivalents because of the amendments or arguments made herein. Examination of the application, and entrance of these amendments, are respectfully requested.

Non-Entrance of Response dated December 11, 2003

The Advisory Action dated January 28, 2004 indicated that the amendment filed December 11, 2003 would not be entered.

The Applicant has amended the claims in this amendment to remove the claim amendments made in the December 11, 2003 amendment. The Applicant respectfully requests that the amendment of December 11, 2003 not be entered, and that the claims presented herein stand as the claims present in the application.

Art-Based Rejections in the Office Action of September 8, 2003

In paragraphs 2-3 of the Office Action, claims 1-2, 4-5, and 8-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaha, et al., USPN 5,763,936, and further in view of Applicant's Admitted Prior Art (AAPA).

In paragraphs 4-5 of the Office Action, claims 6-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaha, et al., USPN 5,763,936, and further in view of Applicant's Admitted Prior Art (AAPA) and further in view of Morita, et al., USPN 5,414,297.

The Applicant respectfully traverses the rejections and submits that the claims are patentable in light of the arguments below.

The Yamaha Reference

The Yamaha reference discloses a semiconductor chip capable of suppressing cracks in the insulating layer. As shown in FIG. 1F, in the chip outer peripheral region, via holes are formed just above the bonding pad lower layer pattern 4a and at the same time, dummy via holes are formed just above the dummy wiring patterns 4b1 to 4b3. See Col. 6, lines 20-23.

The dummy wiring patterns 4b1 to 4b3 of the first wiring layer 4 make the bottom surface of the SOG film 6 formed on the first wiring layer 4 uneven so that the contact area between the SOG film 6 and PECVD SiO2 film 5a increases substantially. The uneven bottom surface of the SOG film 6 (created by the dummy wiring patterns 4b1 to 4b3) disperses the thermal stress at the interface between the SOG film 6 and PECVD SiO2 film 5a, in vertical and horizontal directions relative to the plane of the interface. Therefore, flakes at the interface and cracks in the SOG film 6 to be caused by the flakes can be suppressed. See Col. 9, lines 7-16.

The Applicant's Admitted Prior Art

The AAPA discloses a dummy layer in a dicing region that has a structure similar to the gate structure.

The Morita Reference

The Morita reference discloses a semiconductor device chip with interlayer insulating film covering the scribe lines. An integrated circuit wafer composed of a substrate having a surface carrying a plurality of circuit chips spaced from one another by scribe lines constituted by regions of the substrate surface along which

the substrate will be cut in order to separate the chips from one another, each chip having at least one semiconductor element composed of a plurality of patterned layers of electrically conductive material and the wafer further including at least one interlayer insulation film having portions which extend across each chip and interposed between two of the layers of electrically conductive material to form a component part of each element, the interlayer insulation film further having portions which extend across the scribe lines at the time the substrate is cut along the scribe lines and which are contiguous with portions of the interlayer insulation film that extend across each chip, wherein the wafer is provided with one or more defined patterns located at at least one scribe line region and a passivation film covering the chips and the at least one scribe line region, and each defined pattern is constituted by one of: an observable irregularity in the wafer surface; a film portion of insulating material; or a film portion of electrically conductive material. A strip of electrically conductive material may be disposed in a groove in the interlayer insulation film along each longitudinal edge of each scribe line. See Abstract.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a semiconductor device and method of making a semiconductor device. A device in accordance with the present invention comprises a dicing region provided on a semiconductor substrate to separate a plurality of semiconductor chips each having a gate portion from each other, a plurality of element isolation regions provided on a surface portion of the semiconductor substrate within the dicing region, a plurality of first dummy patterns formed on a surface of the semiconductor substrate so as to correspond to intervals of the plurality of element isolation regions, respectively, and a plurality of

second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy patterns, respectively.

In recent years, Chemical Mechanical Polishing (CMP) is widely used in manufacturing of semiconductor devices. However, CMP causes a film reduction phenomenon called "dishing." As a method for remedying the dishing on the dicing line (also called the scribing line) there is a structure in which laminated film is formed on the dicing line. The prior art disclosed in the present application is a structure in which a film (film 104 of FIG. 1) having the same structure as that of the gate electrode portion on the semiconductor chip is formed as the above laminated film.

In the related art, although the laminated film formed on the dicing line can prevent the dishing, the laminated film causes large waste of the chips due to cracking of the chips when the chip separates from the semiconductor substrate along lines other than the dicing line, or when the laminated film delaminates and causes waste. This waste is called "crack waste."

The present invention avoids generation of a large crack waste, without complicating the manufacturing process, such as adding a step of removing the insulation film which creates a large crack waste. More specifically, as shown in FIGS. 3, 4U, 5, 8, and 9, for example, a plurality of dummy patterns formed on the dicing line remedies dishing, and prevents large cracks of the insulation film by dispersing the stress concentrated in dicing. In other words, the present invention remedies dishing, and minimizes the crack waste generated in dicing by making it easier for the chip to separate along the dicing line.

The Yamaha reference discloses suppression of crack generation, e.g., intrusions of cracks into the chip. In Col. 6, lines 53-55, Yamaha teaches that the

first dummy patterns 4b1 and the second dummy patterns 5b are not formed on the dicing line. Specifically, the first dummy patterns 4b1 and the second dummy patterns 5b are formed in the outer peripheral region of the semiconductor chip. All the insulation film on the dicing line located further outside the dummy patterns is removed in advance, to prevent generation of crack waste in dicing. See FIGS. 1F and 1G.

As such, Yamaha does not teach nor suggest elements formed on the dicing line as in the present invention.

The ancillary references do not remedy the deficiencies of the present invention. Namely, neither the AAPA nor Morita teach nor suggest forming elements on the dicing line as recited in the claims of the present invention.

Thus, it is submitted that independent claims 1 and 11 are patentable over the cited references. Claims 2, 4-10, and 12-13 are also patentable over the cited reference, not only because they contain all of the limitations of the independent claim1, but because claims 2, 4-10, and 12-13 also describe additional novel elements and features that are not described in the prior art. Silence in this response with respect to rejections made in the Office Action is not to be considered acceptance of those rejections.

Conclusion

It is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe that there are matters relating to this continuation application remaining that can be resolved in a telephone interview, the Examiner is urged to call the Applicants' undersigned attorney.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: March 8, 2004

By: _____
Anthony J. Orler
Registration No. 41,232
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701